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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/753,053	12/28/2000	Ravi Kumar Arimilli	AUS920000670US1	9308

7590 09/21/2004

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EXAMINER	
HARKNESS, CHARLES A	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/753,053	ARIMILLI ET AL.	
	Examiner	Art Unit	
	Charles A Harkness	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,17-23 and 25-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-15, 17-23, and 25-28* is/are allowed.

6)☒ Claim(s) *1,8 and 9* is/are rejected.

7)☒ Claim(s) *2-7 and 10-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the amendment to the title, the objection to the specification has been withdrawn.

2. In view of the amendment to claim 11, the 112 rejection to the claim has been withdrawn.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1 and 8 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,625,660; claim 1 of U.S. Patent No. 6,728,873; and claim 1 of U.S. Patent No. 6,691,220.

4. Claim 1 of U.S. Patent No. 6,625,660, claim 1 of U.S. Patent No. 6,691,220, and claim 1 of U.S. Patent No. 6,728,873 contain every element of claims 1 and 8 of the instant application and as such anticipate claims 1 and 8 of the instant application.

5. Claims 9 and 10 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 8 and over claim 12 of U.S. Patent No. 6,691,220.

6. Claim 8 of U.S. Patent No. 6,691,220 and claim 12 of U.S. Patent No. 6,691,220 contain every element of claims 9 and 10 of the instant application and as such anticipate claims 9 and 10 of the instant application.

"A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1 and 8-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Morris et al., U.S. Patent Number 6,286,095 (herein referred to as Morris).

8. Referring to claim 1 Morris has taught a method for full speculation of instruction processing in a multiprocessor data processing system (Morris figures 11-12) comprising:

issuing from a processor a barrier operation on a system bus of said data processing system; and

speculatively executing operations associated with instructions sequentially following said barrier operation in an instruction sequence prior to completion of said barrier operation, wherein operations are speculatively executed relative to a preceding barrier operation whenever the preceding barrier operation has not yet completed (Morris column 4 lines 10-37 column 6 lines 10-27, figure 11; when an ordered store instruction is being executed, a load request from a load instruction would still be speculatively executed).

9. Referring to claim 8 Morris has taught a multiprocessor computer system comprising:

a plurality of processors interconnected by a system bus, wherein said processors including a first processor that speculatively issues load requests and speculatively processes subsequent instructions utilizing data returned by said load request before a completion of a barrier operation that is issued sequentially before said load requests and subsequent instructions, wherein said load request is speculatively issued and said subsequent instructions are speculatively processed relative to the barrier operation such that the speculative issuance and speculative processing are barrier speculative (Morris column 4 lines 10-37, column 6 lines 10-27, figure 11; when an ordered store instruction is being executed, a load request from a load instruction would still be speculatively executed); and

a memory hierarchy connected to said plurality of processors via said system bus that sources said data (Morris column 1 lines 26-42).

10. Referring to claim 9 Morris has taught the multiprocessor computer system of Claim 8, wherein said first processor comprises a load/store unit with logic that controls issuing of load and store instructions before completion of a preceding barrier operation to provide said data to a register of said first processor prior to a return of an acknowledgment for said preceding barrier operations (Morris column 6 lines 10-27, figure 11; since execution of the load instruction took place, the data being loaded in would be stored in the register specified by the instruction).

11. Claims 1 and 8-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Yeager, U.S. Patent Number 6,216,200 (herein referred to as Yeager).

12. Referring to claim 1 Yeager has taught a method for full speculation of instruction processing in a multiprocessor data processing system comprising:

issuing from a processor a barrier operation on a system bus of said data processing system; and

speculatively executing operations associated with instructions sequentially following said barrier operation in an instruction sequence prior to completion of said barrier operation, wherein operations are speculatively executed relative to a preceding barrier operation whenever the preceding barrier operation has not yet completed (Yeager column 23 line 28-column 24 line 3).

13. Referring to claim 8 Yeager has taught a multiprocessor computer system comprising:

a plurality of processors interconnected by a system bus, wherein said processors including a first processor that speculatively issues load requests and speculatively processes subsequent instructions utilizing data returned by said load request before a completion of a

barrier operation that is issued sequentially before said load requests and subsequent instructions, wherein said load request is speculatively issued and said subsequent instructions are speculatively processed relative to the barrier operation such that the speculative issuance and speculative processing are barrier speculative (Yeager column 23 line 28-column 24 line 3); and

a memory hierarchy connected to said plurality of processors via said system bus that sources said data (Yeager figure 1, cache is connected to bus).

14. Referring to claim 9 Yeager has taught the multiprocessor computer system of Claim 8, wherein said first processor comprises a load/store unit with logic that controls issuing of load and store instructions before completion of a preceding barrier operation to provide said data to a register of said first processor prior to a return of an acknowledgment for said preceding barrier operations (Yeager column 5 lines 13-43, column 23 line 28-column 24 line 3; the load/store unit must handle the operations of the load and store instructions as described).

Allowable Subject Matter

15. Claims 2-7 and 11-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

16. Claims 14-15, 17-23, and 25-28 are allowed.

17. Yeager, Morris, Hesson, nor Tran, individually or in combination have taught the limitations of claims 2-7, 10-14, 17-23, and 25-28. In particular, Yeager, Morris, Hesson, nor Tran, have not taught tagging an instruction as being barrier-speculative, where barrier-speculative is defined in Applicants Remarks filed 06/21/04, on the last paragraph of page 13,

where the tag, or flag, is referenced to the speculative instructions subsequently following a barrier operation that has not yet been retired, when those instructions are speculatively executed, or to the results of those operations related to the speculative instructions subsequently following a barrier operation that has not yet been retired. Please see Applicants Remarks filed 06/21/04, pages 13 and 15-16.

Response to Arguments

18. Applicant's arguments filed 06/21/04 have been fully considered but they are not persuasive.

19. Applicant argue, in respect to the rejection of claims 1 and 8:

> "Morris teaches the exact opposite of the functionality provided by Applicants' invention."

20. This is not persuasive. Referring to Morris (column 4 lines 10-37, column 6 lines 10-27, figure 11), Morris teaches that when mailbox store instruction, or barrier instruction, is being executed, a load request from a load instruction would still be speculatively executed. Although Morris does not teach the whole invention of the instant application as described by the specification, Morris does teach the limitations of claims 1 and 8-9 as presented.

21. Applicant's arguments, filed 06/21/04, with respect to the rejections of claims 10-11, 14-15, 17, 22-23, and 25 have been fully considered and are persuasive. The 103 rejections of claims 10-11, 14-15, 17, 22-23, and 25 have been withdrawn. Please see Applicants Remarks filed 06/21/04, pages 15-16.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579 and 571-272-4167 after 10/12/04. The examiner can normally be reached on 8Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Charles Allen Harkness

Examiner

Art Unit 2183

September 15, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100